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SPECIFICATION

METHOD FOR SHIELDING LOGIC SIGNALS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to electronic systems utilizing logic signals. More particularly, the present invention provides a method for shielding signal lines which would otherwise inductively or capacitively couple to adjacent conductors.

2. The Background Art

As integrated circuit (IC) designs become more complex, and as those designs utilize higher signal frequencies, there is an increased likelihood of crosstalk between adjacent interconnect lines within one or more functional blocks in an IC.

Typical IC's include large and small functional blocks coupled together by interconnect lines.

FIG. 1 is a block diagram of a prior art IC showing megablocks and interconnect lines.

Referring to FIG. 1, integrated circuit 10 comprises megablocks 12, 14, 16, 18, and 20, each megablock being connected to other megablocks by interconnect lines 22a through 22i provided for that purpose. Each of megablocks 12, 14, 16, 18, and 20 includes logic gates, transistors, and other components. It is common for IC's to include megablocks which have rows of functional circuits, with the circuitry within one or more rows being connected to circuitry in other rows by interconnects which are located in tracks. A track is a location on an integrated circuit die in which an interconnect may be placed, depending on a given design.

FIG. 2 depicts a typical layout of a prior art megablock showing power, ground, and possible track locations.

Referring to FIG. 2, megablock 30 comprises power conductors 32a through 32h provided therein to supply power to columns of bit slices 36a through 36h, and ground conductors 34a through 34h. In a typical megablock, each row such as rows 38 and 40 might have similar functional circuitry throughout each of the bit slices, with the functional circuitry in a given bit slice being connected to circuitry in a different row.

FIG. 3 depicts a prior art bit slice in any given row within a megablock.

Referring to FIG. 3, bit slice 40 comprises power conductor 42, ground conductor 44, dotted lines showing potential track locations 46, 48, and 50, and conductors 52 and 54. In a typical bit slice, there are many more signal paths which connect various functional blocks together in order to perform the intended function. However, only two signal paths are depicted herein in order to avoid needlessly overcomplicating the disclosure and drawings.

As circuit designs become more complex, and utilize higher and higher signal frequencies, the distance between conductors becomes an increasingly

critical factor due to the possibility that signals on one conductors might be inductively or capacitively coupled to one or more other conductors. For example, conductor 52 is adjacent to conductor 54, making it possible that a signal on conductor 54 might be unintentionally coupled to conductor 52, causing conductor 52 to act in a way which is not intended by the designer.

In order to understand how the prior art routes conductors so that unintended coupling between conductors is minimized, it is necessary to understand how integrated circuits are designed.

Typically, circuitry functionality is modeled in a high-level language such as Verilog. The model is then provided to an analyzer which determines the placement of functional blocks and the routing of circuitry, so that the intended design functions as modeled. Thus, although the designer determines the input and output conditions necessary for proper functionality of a system, the placement of conductors such as conductors 52 and 54 in a single bit slice such as depicted in FIG. 2 is determined using design rules. These design rules include

details specifically associated with the manufacturing process which will be used to manufacture the IC.

One element of a design which is controllable, and which also affects the placement of conductors in a bit slice is whether a given signal path requires a "quiet" environment in which to operate. If a given signal path is required to be placed in an environment where inductive and capacitive coupling is minimized, the designer provides that information in the model supplied to the analyzer, and the analyzer takes appropriate action to maximize the coupling of the sensitive conductor to a constant signal source. The appropriate prior art action is to add a new conductor.

For example, in FIG. 4, sensitive conductor 52 has been placed by the analyzer in the location depicted, immediately adjacent to noisy conductor 54. In order to minimize the coupling between conductor 52 and conductor 54, prior art analyzers route a third conductor 60 from a stable conductor, such as ground conductor 44, to a position adjacent to conductor 52.

This technique for routing a constant conductor is known to those of ordinary skill in the art to cause a sensitive conductor to partially couple to the constant conductor, thus minimizing the coupling of the sensitive conductor to the noisy conductor. However, this technique also mandates the use of an available track within a bit slice for the placement of the extra conductor, making the use of that track for other circuitry impossible. In order to provide enough silicon real estate to accomplish this technique in crowded bit slices, it is often necessary to design the wafer to allow for larger bit slices, an undesirable effect.

While the methods used in the prior art are effective for minimizing the inductive and capacitive coupling of noisy signal paths to sensitive signal paths, prior art methods suffer in that significant unnecessary use of silicon real estate results from those methods.

It would therefore be beneficial to provide a method for minimizing coupling of noisy conductors to sensitive conductors which utilizes less silicon real estate than the prior art.

SUMMARY OF THE INVENTION

A method for routing conductors in an integrated circuit design is disclosed, including the steps of determining the number of sensitive conductors requiring placement into quiet track locations, wherein a quiet track location is defined as any track location immediately adjacent to a stable conductor, determining the number of quiet track locations available in said integrated circuit design, and routing one or more sensitive conductors into one or more quiet track locations.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a prior art IC showing megablocks and interconnect lines.

FIG. 2 depicts a typical layout of a prior art megablock showing power, ground, and possible track locations.

FIG. 3 depicts a prior art bit slice in any given row within a megablock.

FIG. 4 depicts the prior art bit slice of FIG. 3 further including a quieting conductor.

FIG. 5 depicts a present invention bit slice having conductors routed according to one embodiment of the present invention.

FIG. 6 is a side view of a bit slice of an integrated circuit showing preferred tracks for the placement of sensitive conductors.

FIG. 7 is a flow chart showing steps in a method of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

In this disclosure, a stable conductor shall generally refer to a conductor which does not change state. The examples used in this disclosure of stable conductors are power and ground. However, those of ordinary skill in the art will

readily recognize that other stable conductors fitting this description exist in the art.

FIG. 5 depicts a bit slice having conductors routed according to one embodiment of the present invention.

Referring to FIG. 5, noisy conductor 54 is placed as previously seen in FIG 3. However, conductor 62, a conductor determined to be critically sensitive, has been placed immediately adjacent to stable ground conductor 44. Noisy conductor 64 although adjacent to conductor 62 does not inductively couple to conductor 62 due to the "quieting" influence on conductor 62 by ground conductor 44.

Because integrated circuits are constructed using multiple metal layers, the quieting influence on a conductor by a stable conductor is not restricted to a single metal layer. Therefore, so long as a sensitive conductor needing a quiet environment is designed to be placed at a track location immediately adjacent to a stable conductor, the effects of the quieting influence of the stable conductor may be felt.

FIG. 6 is a side view of a bit slice of an integrated circuit showing preferred tracks for the placement of sensitive conductors.

Referring to FIG. 6, bit slice 70 includes two metal layers 72 and 74, with each of layers 72 and 74 including a power conductor 42 and a ground conductor 44. According to one embodiment of the present invention, "quiet" locations for the placement of sensitive conductors include tracks 76a through 76h. These tracks are all immediately adjacent to stable conductors.

Tracks such as track 76a, which are immediately adjacent to more than one stable conductor, are considered to be especially quiet, due to the increased coupling to more than one stable conductor. Therefore, tracks 76a, 76c, 76f and 76g are especially quiet, and should be utilized for placement of the most sensitive conductors, as determined by the IC designer. An IC may have four or more metal layers, providing for potential quiet tracks above, below, left, and right of a given stable conductor.

FIG. 7 is a flow chart showing steps in a method according to the present invention.

Referring to FIG. 7, the method begins at step 80 wherein the signal conductors which need a quiet environment in which to operate are prioritized. At this step, if a given design is known to have fewer sensitive lines than preferred tracks to place them, all sensitive conductors may be routed into a preferred location. Alternatively, a designer may rank each sensitive conductor in order of its importance relative to other sensitive conductors. In this alternative case, conductors are routed according to their rank, thus ensuring that the more highly ranked conductors are placed in quiet track locations.

At step 82, it is determined how many preferred tracks exist in the present design. At this step, the analyzer may alternatively rank the preferred tracks, ranking the tracks which are immediately adjacent to two stable conductors higher than tracks which are immediately adjacent to a single stable conductor.

At step 84, the analyzer routes sensitive conductors into tracks previously designated at step 82. If, at step 80, the designer had ranked sensitive conductors according to the desirability of placing them in a stable location, the analyzer routes the higher ranked conductors first. If, at step 82, the analyzer had ranked the preferred tracks according to whether any given preferred track had one, two, or more adjacent stable conductors, the analyzer, at step 84, places the most highly ranked sensitive conductor at the most preferred location. The analyzer then places the next highest ranked sensitive conductor at the next most preferred track location, and so on, until all ranked conductors have been placed.

At step 86, the analyzer routes any conductors not already routed into the remaining track locations.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.